

EXPERIMENT REPORT

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| **Experiment Name** | Logic Gates and Multivibrators |
| **Lab Assistant** | Atilla Uygur |
| **Author of the Report (Name / No / Department)** | Tuğrul YATAĞAN  040100117  Computer Engineering |
| **Group Number and**  **Experiment Date** | D27  13.12.2013 |

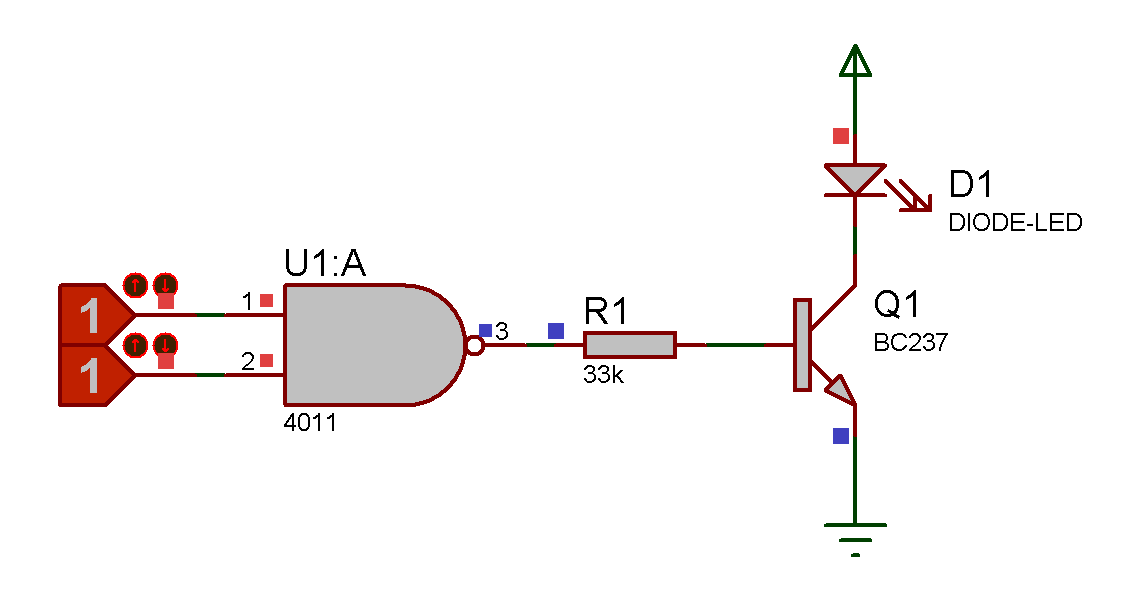
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| **Report Score** | **Deliver Date** | **Receive Date** |
|  | 20.12.2013 |  |

### Aim of the Experiment

In this experiment session, we investigate basic understanding of the basic logic gates and the principle of operations for monostable and bistable circuits.

### Exp #1 Circuit for NAND gate

We built the following circuit with a NAND gate, a resistor, a LED and a BJT pnp transistor. Than we investigate the states by LED with corresponding inputs. BJT transistor is used for obtaining adequate current flow for LED. Only the NAND gate’s outputs cannot give enough current for LED. BJT works on saturated region or cutoff according to NAND gate’s input.

Here is a circuit of the experiment on simulation program:****

We obtain the following truth table by observing during the experiment:

|  |  |  |
| --- | --- | --- |
| **NAND Gate** | | |
| **A** | **B** | **O** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

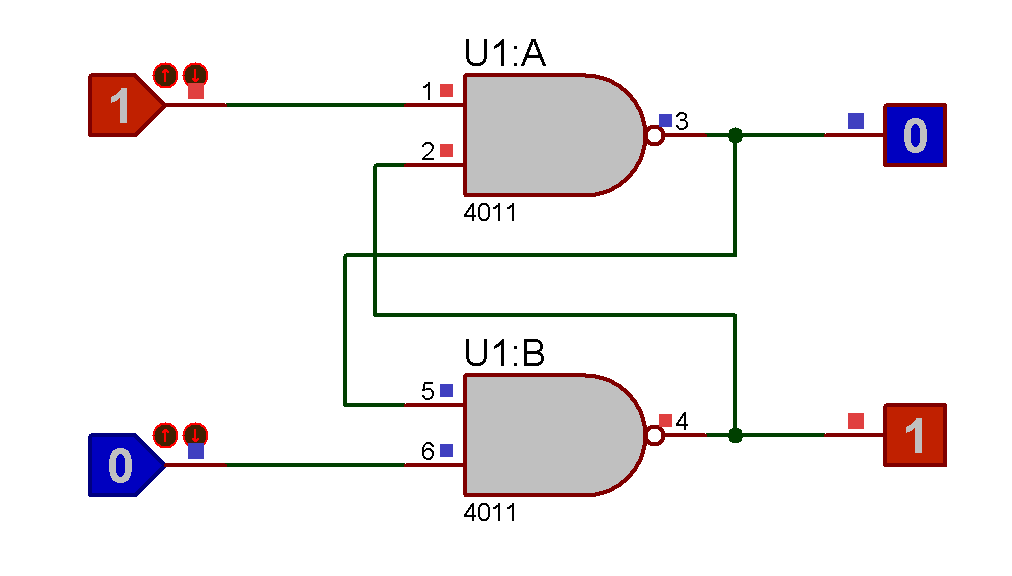
Truth Table

O =

### Exp #2 SR Latch

We built the following circuit with two NAND gates and we connect inputs to switches, outputs to LED’s on Cadet Experiment set. Than we start to investigate the states by LEDs with corresponding inputs and previous states.

Here is a circuit of the experiment on simulation program:



We obtain the following truth table by observing during the experiment:

|  |  |  |  |
| --- | --- | --- | --- |
| **SR Latch** | | | |
| **S** | **R** | **Q** | **Q’** |
| 0 | 0 | - | - |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | Q0 | Q0’ |

Truth Table

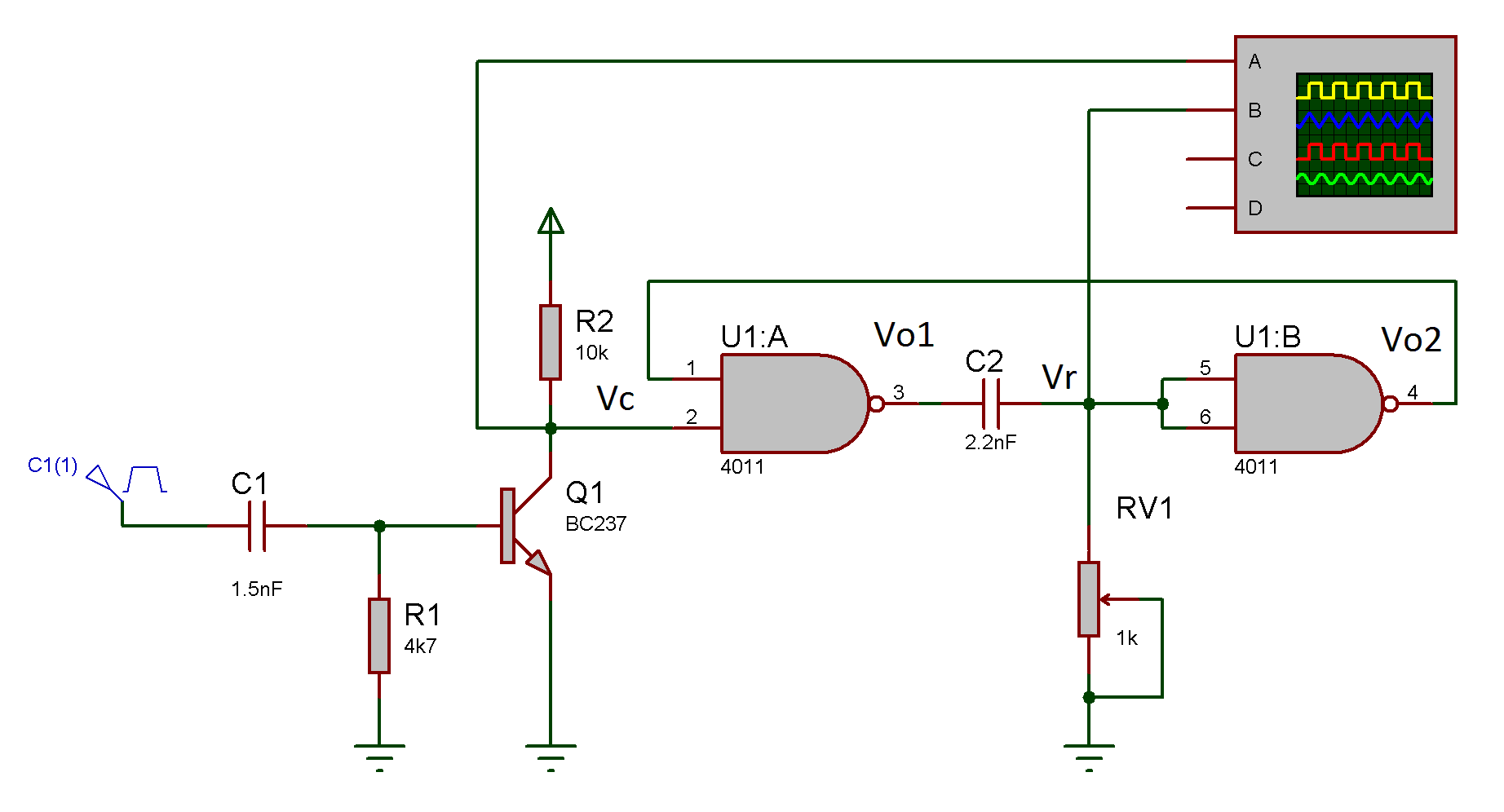
When set and reset pins are both 0 the outputs will be unstable so giving S=0 and R=0 inputs at same time is illegal operation for SR latch.

### Exp #3 Monostable Multivibrator

In this experiment we investigated the monostable multivibrators. We built the following circuit with two NAND gates, a 4.7KΩ resistor, a 4potantiometer, a 1.5nF capacitor, a 2.2nF capacitor, a BJT pnp transistor and square wave generator.

We applied 5V square wave signal at the input and observed the Vc and Vr voltage shapes by the oscilloscope.

Here is a circuit of the experiment on simulation program:



Second NAND gate behaves as NOT gate in this circuit. O = =

Observation of (V-t) graphic at the BJT’s collector pin (Vc) on oscilloscope screen:

V

5V

t

Observation of (V-t) graphic at the second NAND gate’s input pin (Vr) on oscilloscope screen:

4V

2V

V

t

-0.7V

When we give the square wave at the input and the top of the wave is come, transistor starts to transmission and Vc will be logical 0. Because of first NAND gate’s inputs are 0, VO1 will be logical 1. These gates are CMOS circuits so change at the outputs are sharp. But 2.2nF capacitor is not fast as CMOS gates, so it cannot reacts quickly and voltages between capacitor’s terminals cannot quickly decreases, Vx will be logical 1. When the Vx is logical 1, second NAND gate’s output VO2 and first NAND gate’s upper inputs will be logical 1. During these conditions even Vin becomes logical 0, circuit will keep its conditions. A current flow over potentiometer and Vx voltage’s drops cause of VX is logical 1 in this condition. If the resistance on potentiometer is high this current will be small and the circuit is preserves its condition longer. Also the charging time of capacitor will be longer. So resistance of potentiometer determines charging and discharging time of capacitor. When the Vx voltage becomes lower than the threshold value of VDD/2, second NAND’s inputs will be logical 0, so second NAND’s output will be logical 0. But again capacitor will not be able to responds these changes quickly and tries to preserves its conditions. When VO1 is logical 0, Vx tries to drop to –VDD/2, but diodes inside the NAND gates will not permit these voltages so Vx will remain at diodes threshold voltages. Eventually Vx will never be -2.5V, instead it will be about -0.7V. These diodes also prevent static electricity’s sudden changes cause by human factors.

Experiment results, measurements and oscilloscope outputs are stated in the protocol paper during experiment.